DEVELOPMENT OF SINGLE PHASE PWM INVERTER FOR UPS APPLICATION

MOHAMMAD ARIFF BIN YAAKOB

This thesis is submitted as partial fulfillment of the requirement for the award of the Bachelor Degree Electrical Engineering (Power System)

Faculty of Electrical & Electronic Engineering
Universiti Malaysia Pahang

NOVEMBER, 2007

ABSTRACT

This project is to develop an inverter circuit for Uninterruptable Power Supply (UPS) application. Inverters are circuit that convert DC to AC. The function of inverter is to create an AC voltage by using a DC voltage source and in UPS system, the voltage source that used DC voltage commonly batteries. Pulse-width modulation (PWM) technique is use in this project because with PWM, the amplitude of the output voltage can be controlled with the modulating waveforms. In this project, Metal Oxide Field Effect Transistor (MOSFET) is used as switch in the full bridge inverter circuit design. For alternated control purpose, sequential switching is designed for PWM get-way through the MOSFET driver. The function of the driver is to control the ON/OFF of the MOSFET. Driver of the MOSFET is essential in the inverter circuit because the driver use to interface between control circuits (low voltage) and inverter circuit (high voltage). The objective of this project is to develop single phase PWM Inverter for UPS application and to design the circuit, simulate and analyze the switching characteristic of single phase PWM inverter. The simulation of full-bridge single phase inverter for this project has been done by using Unipolar scheme and the output waveform is successfully generated. The switching process in hardware is control by PIC 16F877a and the MOSFET driver is using IR2110. At the end of this project, the results from simulation were compared with hardware.

CHAPTER 1

INTRODUCTION

1.1 Background

This chapter explains briefly about Inverter and its operation. This chapter also explains the overview of project objectives, scopes and thesis outline.

1.2 Overview of Inverter Project

Inverters are circuits that convert DC to AC. More precisely, inverters transfer power from a DC source to an AC load. The function of inverter is to create an AC voltage by using a DC voltage source and in UPS system, the voltage source that used DC voltage commonly batteries. Inverters are used in applications such as adjustable-speed AC motor drives, uninterruptable power supplies (UPS), and AC appliances run from an automobile battery.

In this report, a design for a power inverter circuit is presented for conversion of energy from DC battery to AC power to be used mainly for Uninterruptable Power Supply (UPS) applications. The configuration is achieved using a full-bridge PWM

inverter. DC-DC converter circuit not been constructed in this project and DC supply from High voltage DC supply been used.

In this project, PIC microcontroller used to control the output by using sinusoidal pulse width modulation technique based on open loop configuration system. The proposed practical circuit operates from a 340V DC input and outputs a regulated 240V AC, 50Hz voltage. A complete circuit analysis, design and cost evaluation is presented and supported by PSPICE simulation results.

1.3 Objective

The objective of this project is to develop single phase PWM Inverter for UPS application. In this part, the development of PWM Inverter circuit is the main task of this project to convert DC power from battery to AC. These projects also develop an open-loop control system by using PIC microcontroller to control output voltage. The other objectives of this project are to design the circuit, simulate and analyze the switching characteristic of single phase PWM inverter.

1.4 Scope of the Project

The main scopes of this project are;

i. Design PWM Inverter circuit that generates $240V_{RMS,}$ 50Hz and 500W of power.
ii. Microcontroller used as a controller to control switching process. The type of PIC used is PIC16F877.
iii. ORCAD PSpice and Multisim PSpice program are used to simulate and design the circuit.

CHAPTER 2

THEORY AND LITERATURE REVIEW

2.1 Uninterruptible Power Supply (UPS)

Figure 2.1: Small UPS

An uninterruptible power supply (UPS), uninterruptible power source or sometimes called a battery backup is a device which maintains a continuous supply of electric power to connected equipment by supplying power from a separate source when utility power is not available [1].

A UPS is inserted between the source of power (typically commercial utility power) and the load it is protecting. When a power failure or abnormality occurs, the UPS will effectively switch from utility power to its own power source almost instantaneously [1].

While not limited to any particular type of equipment, a UPS is typically used to protect computers, telecommunication equipment or other electrical equipment where an unexpected power disruption could cause injuries, fatalities, serious business disruption or data loss. UPS units come in sizes ranging from units which will back up a single computer without monitor (around 200 VA) to units which will power entire data centers or buildings (several megawatts). Larger UPS units typically work in conjunction with generators [1].

Historically, UPS were very expensive and were most likely to be used on expensive computer systems and in areas where the power supply is interrupted frequently. However, UPS units are now more affordable, and have become an essential piece of equipment for data centers and business computers, but are also used for personal computers, entertainment systems and more [1].

In certain countries, where the electrical grid is under strain, providers struggle to ensure supply during times of peak demand (such as summer, during which air-conditioning usage increases). In order to prevent blackouts, electrical utilities will sometimes use a process called rolling blackouts or load shedding, which involves cutting the power to large groups of customers for short periods of time. Several major blackouts occurred in 2003, most notably the 2003 North America blackout in the north-eastern US and eastern Canada and the 2003 Italy blackout, both of which affected over 50 million people, and brought attention to the need for UPS power backup units [1].

A UPS is not to be confused with a standby generator, which does not provide protection from a momentary power interruption and may result in an interruption when it is switched into service, whether manually or automatically. However, such generators are typically placed before the UPS to provide cover for lengthy outages [1].

2.2 Microcontroller (PIC 16F877A).

PIC is a family of Harvard architecture microcontrollers made by Microchip Technology, derived from the PIC1650 originally developed by General Instrument's Microelectronics Division. The name PIC was originally an acronym for "**Programmable Intelligent Computer**".

Figure 2.2: PIC16F8777A

In this project, a microcontroller; PIC16F877a (Figure 2.2) is use to control the output. The reason for use microcontroller is the PIC architecture is distinctively minimalist. It is characterized by the following features:

- separate code and data spaces
- a small number of fixed length instructions
- most instructions are single cycle execution (4 clock cycles), with single delay cycles upon branches and skips

- a single accumulator (W), the use of which (as source operand) is implied
- All RAM locations function as registers as both source and/or destination of math and other functions.
- data space mapped CPU, port, and peripheral registers
- the program counter is also mapped into the data space and writable (this is used to synthesize indirect jumps)
- 10-bit multi-channel Analog-to-Digital converter
- has 33 input or output ports (see Figure 2.3)

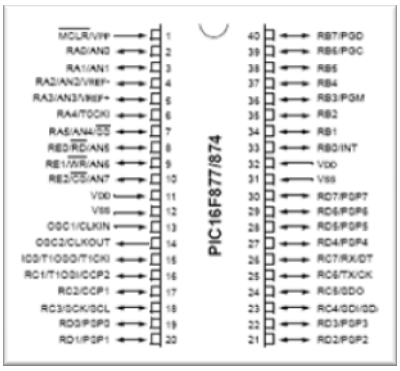

Figure 2.3: PIC Schematic

Unlike most other CPUs, there is no distinction between "memory" and "register" space because the ram serves the job of both memory and registers, and the ram is usually just referred to as the register file or simply as the registers.

PIC microcontroller have a very small set of instructions (only 35 instruction), leading some to consider them as RISC devices, however many salient features of RISC CPU's are not reflected in the PIC architecture. For example:

- it does not have load-store architecture, as memory is directly referenced in arithmetic and logic operations
- it has a singleton working register, whereas most modern architectures have significantly more

PIC have a set of register files that function as general purpose RAM, special purpose control registers for on-chip hardware resources are also mapped into the data space. The addressability of memory varies depending on device series, and all PIC devices have some banking mechanism to extend the addressing to additional memory. Later series of devices feature move instructions which can cover the whole addressable space, independent of the selected bank. In earlier devices (ie. the baseline and mid-range cores), any register move had to be through the accumulator.

To synthesize indirect addressing, a "file select register" (FSR) and "indirect register" (INDF) are used: A read or write to INDF will be to the memory pointed to by FSR. Later devices extended this concept with post and pre increment/decrement for greater efficiency in accessing sequentially stored data. This also allows FSR to be treated like a stack pointer.

All PICs feature Harvard architecture, so the code space and the data space are separate. PIC code space is generally implemented as EPROM, ROM, or FLASH ROM. In general, external code memory is not directly addressable due to the lack of an external memory interface.

The PIC architecture has no (or very meager) hardware support for saving processor state when servicing interrupts. The 18 series improved this situation by implementing shadow registers which save several important registers during an interrupt. The PIC architecture may be criticized on a few important points.

- The few instructions, limited addressing modes, code obfuscations due to the "skip" instruction and accumulator register passing makes it difficult to program in assembly language, and resulting code difficult to comprehend. This drawback has been alleviated by the increasing availability of high level language compilers.

- Data stored in program memory is space inefficient and/or time consuming to access, as it is not directly addressable.

2.3 HV Floating MOS-Gate Driver IC

2.3.1 Gate Drive Requirements of High-Side Devices

The gate drive requirements for a power MOSFET or IGBT utilized as a high-side switch (the drain is connected to the high voltage rail, as shown in Figure 2.4) driven in full enhancement (i.e., lowest voltage drop across its terminals) can be summarized as follows:

1. Gate voltage must be 10 V to 15 V higher than the drain voltage. Being a high-side switch, such gate voltage would have to be higher than the rail voltage, which is frequently the highest voltage available in the system.

2. The gate voltage must be controllable from the logic, which is normally referenced to ground. Thus, the control signals have to be level-shifted to the source of the high-side power device, which, in most applications, swings between the two rails.

3. The power absorbed by the gate drive circuitry should not significantly affect the overall efficiency.

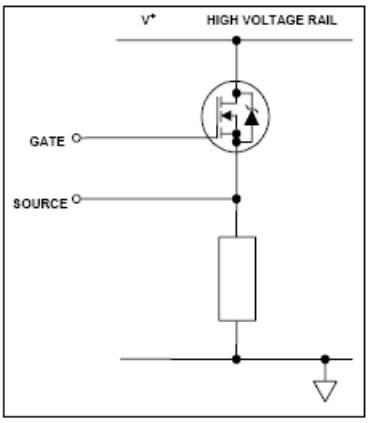

Figure 2.4: Power MOSFET in the High-Side Configuration

With these constraints in mind, several techniques are presently used to perform this function. Each basic circuit can be implemented in a wide variety of configurations [2].

International Rectifier's family of MOS-gate drivers (MGDs) integrate most of the functions required to drive one high-side and one low-side power MOSFET or IGBT in a compact, high performance package. With the addition of few components, they provide very fast switching speeds and low power dissipation. They can operate on the bootstrap principle or with a floating power supply. Used in the bootstrap mode, they can operate in most applications from frequencies in the tens of Hz up to hundreds of kHz [2].

2.3.2 Low-Side Channel

The driver's output stage is implemented either with two n-channel MOSFETs in the totem pole configuration (source follower as a current source and common source for current sinking), or with an n-channel and a p-channel CMOS inverter stage. Each MOSFET can sink or source gate currents from 0.12 A to 4 A, depending on the MGD. The source of the lower driver is independently brought out

to the COM pin so that a direct connection can be made to the source of the power device for the return of the gate drive current. An under voltage lockout prevents either channel from operating if V_{CC} is below the specified value (typically 8.6/8.2 V) [2].

Any pulse that is present at the input pin for the low-side channel when the UV lockout is released turns on the power transistor from the moment the UV lockout is released. This behavior is different from that of the high-side channel [2].

2.3.3 High-Side Channel

This channel has been built into an "isolation tub" capable of floating from 500 V or 1200 V to -5 V with respect to power ground (COM). The tub "floats" at the potential of V_S. Typically this pin is connected to the source of the high-side device, as shown in Figure 2 and swings with it between the two rails [2].

If an isolated supply is connected between V_B and V_S, the high-side channel will switch the output (HO) between the positive of this supply and its ground in accordance with the input command [2].

One significant feature of MOS-gated transistors is their capacitive input characteristic (i.e., the fact that they are turned on by supplying a charge to the gate rather than a continuous current). If the high-side channel is driving one such device, the isolated supply can be replaced by a bootstrap capacitor (C_{BOOT}) [2].

The gate charge for the high-side MOSFET is provided by the bootstrap capacitor which is charged by the 15 V supply through the bootstrap diode during the

time when the device is off (assuming that V_S swings to ground during that time, as it does in most applications). Since the capacitor is charged from a low voltage source the power consumed to drive the gate is small. The input commands for the high-side channel have to be level-shifted from the level of COM to whatever potential the tub is floating at which can be as high as 1200 V. As shown in Figure 2 the on/off commands are transmitted in the form of narrow pulses at the rising and falling edges of the input command. They are latched by a set/reset flip-flop referenced to the floating potential [2].

The use of pulses greatly reduces the power dissipation associated with the level translation. The pulse discriminator filters the set/reset pulses from fast dv/dt transients appearing on the V_S node so that switching rates as high as 50 V/ns in the power devices will not adversely affect the operation of the MGD. This channel has its own under voltage lockout (on some MGDs) which blocks the gate drive if the voltage between V_B and V_S (i.e., the voltage across the upper totem pole) is below its limits. The operation of the UV lockout differs from the one on V_{CC} in one detail: the first pulse *after* the UV lockout has released the channel changes the state of the output. The high voltage level translator circuit is designed to function properly even when the V_S node swings below the COM pin by a voltage indicated in the datasheet (typically 5 V). This occurs due to the forward recovery of the lower power diode or to the LdI/dt induced voltage transient [2].

2.3.4 How to Select the Bootstrap Components

The bootstrap diode and capacitor are the only external components strictly required for operation in a standard PWM application. Local decoupling capacitors on the V_{CC} (and digital) supply are useful in practice to compensate for the inductance of the supply lines [3].

The voltage seen by the bootstrap capacitor is the V_{CC} supply only. Its capacitance is determined by the following constraints:

1. Gate voltage required to enhance MGT
2. I_{QBS} - quiescent current for the high-side driver circuitry
3. Currents within the level shifter of the control IC
4. MGT gate-source forward leakage current
5. Bootstrap capacitor leakage current

Factor 5 is only relevant if the bootstrap capacitor is an electrolytic capacitor, and can be ignored if other types of capacitor are used. Therefore it is always better to use a non-electrolytic capacitor if possible [3].

The minimum bootstrap capacitor value can be calculated from the following equation:

$$C \geq \frac{2\left[2Q_g + \frac{I_{qbs(max)}}{f} + Q_{ls} + \frac{I_{Cbs(leak)}}{f}\right]}{V_{cc} - V_f - V_{LS} - V_{min}} \qquad (2.1)$$

Where:

Q_g = Gate charge of high-side FET

f = frequency of operation

$I_{Cbs\ (leak\ )}$ = bootstrap capacitor leakage current

$I_{qbs\ (max)}$ = Maximum VBS quiescent current

V_{CC} = Logic section voltage source

V_f = Forward voltage drop across the bootstrap diode

V_{LS} = Voltage drop across the low-side FET or load

V_{Min} = Minimum voltage between VB and VS.

Q_{ls} = level shift charge required per cycle (typically 5 nC for 500 V/600 V MGDs and 20 nC for 1200 V MGDs)

The bootstrap diode must be able to block the full voltage, this occurs when the top device is on and is about equal to the voltage across the power rail. The current rating of the diode is the product of gate charge times switching frequency. For an IRF450 HEXFET power MOSFET operating at 100 kHz it is approximately 12 mA [3].

The high temperature reverse leakage characteristic of this diode can be an important parameter in those applications where the capacitor has to hold the charge for a prolonged period of time. For the same reason it is important that this diode have an ultra-fast recovery to reduce the amount of charge that is fed back from the bootstrap capacitor into the supply [3].

2.3.5 How to Deal With Negative Transients on the V_s Pin

Of the problems caused by parasitics, one of the main issues for control ICs is a tendency for the V_S node to undershoot the ground following switching events. Conversely, overshoot does not generally present a problem due to the high differential voltage capability of International Rectifier's proven HVIC process [2].

International Rectifier's control ICs are guaranteed to be completely immune to V_S undershoot of at least 5 V, measured with respect to COM. If undershoot exceeds this level, the high-side output will temporarily latch in its current state. Provided V_S remains within absolute maximum limits the IC will not suffer damage, however the high-side output buffer will not respond to input transitions while undershoot persists beyond 5 V. This mode should be noted but proves trivial in most applications, as the high-side is not usually required to change state immediately following a switching event [2].

The signals listed below should be observed both in normal operation and during high-stress events such as short circuit or over-current shutdown, when di/dt is highest. Readings should always be taken directly across IC pins as shown in Figure 2.5, so that contributions from the parasitics in the drive coupling are included in the measurement [2].

(1) High-side offset with respect to common; V_S-COM

(2) The floating supply; V_B - V_S

The following guidelines represent good practice in control IC circuits and warrant attention regardless of the observed latch-up safety margin [2].

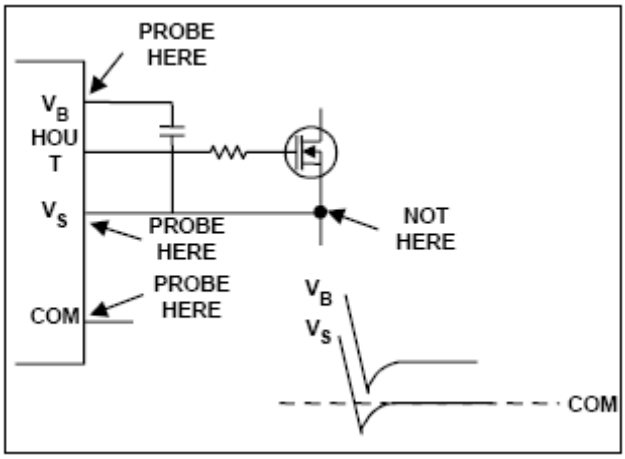

Figure 2.5: Considering the V_S Spike during the Reverse Recovery

2.3.6 Minimize the Parasitics

1) Use thick, direct tracks between switches with no loops or deviation.
2) Avoid interconnect links. These can add significant inductance.
3) Reduce the effect of lead-inductance by lowering package height above the PCB.
4) Consider co-locating both power switches to reduce track lengths.

2.3.7 Reduce Control IC Exposure

1) Connect V_S and COM as shown in Figure 2.6.
2) Minimize parasitics in the gate drive circuit by using short, direct tracks.
3) Locate the control IC as close as possible to the power switches.

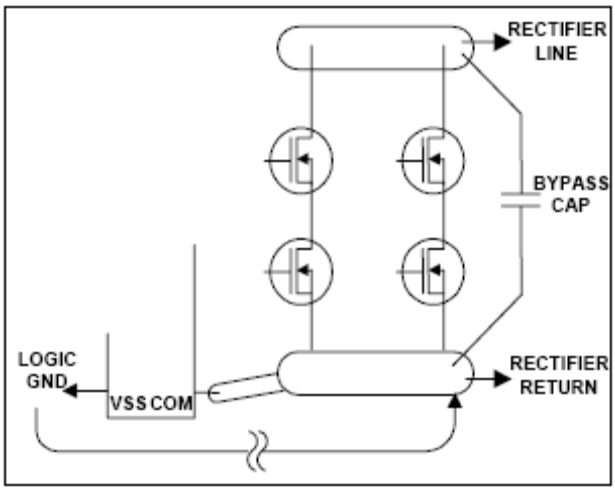

Figure 2.6: Ground Connections and Layout

2.3.8 Improve Local Decoupling

1) Increase the bootstrap capacitor (C_B) value to above 0.47 µF using at least one low-ESR capacitor. This will reduce overcharging from severe V_S undershoot.
2) Use a second low-ESR capacitor from V_{CC} to COM. As this capacitor supports both the low-side output buffer and bootstrap recharge, we recommend a value at least ten times higher than C_B.
3) Connect decoupling capacitors directly across the appropriate pins as shown in Figure 2.7.
4) If a resistor is needed in series with the bootstrap diode, verify that V_B does not

fall below COM, especially during start-up and extremes of frequency and duty cycle.

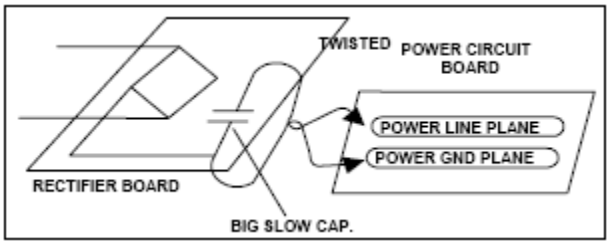

Figure 2.7: Power Bypass Capacitor

Granted proper application of the above guidelines, the effects of V_S undershoot will be minimized at source. If the level of undershoot is still considered too high, then some reduction of dv/dt may be necessary [2].

External snubbing and/or increasing gate drive resistance may be used to trade efficiency for lower switching rate. If the system will not tolerate this, then fast anti-parallel clamping diodes may be considered appropriate. HEXFRED diodes are ideal for this purpose [2].

2.4 Inverter

2.4.1 Power Inverter

A power inverter is a device that converts DC (Direct Current) power into AC (Alternating Current) power. The AC output is usually 120 VAC, 60 Hz (USA domestic power) or 230 VAC, 50 Hz (International power). Aircraft applications often require 115 VAC, 400 Hz. Nova Electric offers all three of these common output voltages, in both single and three-phase configurations, as well as other special / custom outputs [4].

2.4.2 Inverter Applications

With a large enough battery bank, or a large enough alternator output from a vehicle, almost anything within reason can be operated from a power inverter – this assumes that the inverter has the proper power output for the given load. Everyday appliances such as microwaves, power tools, TVs and VCRs, lights, audio/visual equipment, battery chargers and computers are common loads. An inverter sized for loads with heavy inrush current can be used to power air compressors, water pumps, heaters, ventilation fans, and air conditioners. Nova Electric's Pure Sine Wave inverters are ideal for running sensitive test equipment such as communications equipment, oscilloscopes, scales, high end stereos & video equipment, communications equipment, etc [4].

2.4.3 Types of Inverter

Square Wave: Square Wave units could be harmful to some electronic equipment, especially equipment with transformers or motors. The square wave output has a high harmonic content which can lead such equipment components to overheat Square Wave units were the pioneers of inverter development and, like the horse and buggy, are no longer relevant for modern use [4].

Modified Square Wave: The most common, general-use inverters available are "Modified Sine Wave". Usually available at more moderate pricing compared to pure sine wave models. Modified Square Wave (or "Modified Sine Wave" and "Quasi Sine Wave") output inverters are designed to have somewhat better characteristics than Square Wave units, while still being relatively inexpensive. Although designed emulate a Pure Sine Wave output, Modified Square Wave inverters do not offer the same perfect electrical output. As such, a negative by-product of Modified output units is electrical

noise, which can prevent these inverters from properly powering certain loads. For example, many TVs and stereos use power supplies incapable of eliminating common mode noise. As a result, powering such equipment with a Modified Square Wave may cause a "grain" or small amount of "snow" on your video picture, or "hum" on your sound system. Likewise, most appliances with timing devices, light dimmers, battery chargers, and variable speed devices may not work well, or indeed, may not work at all [4].

Pure Sine Wave: Pure or True Sine Wave inverters provide electrical power similar to the utility power you receive from the outlets in your home or office, which is highly reliable and does not produce electrical noise interference associated with the other types of inverters. With its "perfect" sine wave output, the power produced by the inverter fully assures that your sensitive loads will be correctly powered, with no interference. Some appliances which are likely to require Pure Sine Wave include computers, digital clocks, battery chargers, light dimmers, variable speed motors, and audio/visual equipment. If your application is an important video presentation at work, opera on your expensive sound system, surveillance video, a telecommunications application, any calibrated measuring equipment, or any other sensitive load, you must use a Pure Sine Wave inverter [4].

2.4.4 Basic Half-Bridge Inverter Circuit Resistive Load

To illustrate the basic concept of a DC-to-AC inverter circuit we consider a half-bridge voltage-source inverter circuit under resistive load as shown in Fig. 2.8 (a). Its switching waveforms for S1, S2 and the result output voltage are shown in Fig. 2.8 (b).

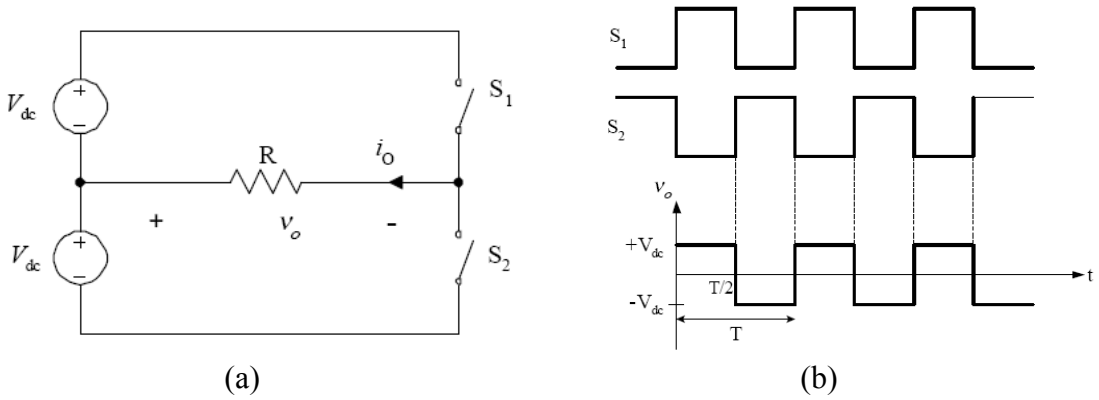

Figure 2.8: (a) Half-bridge Inverter under resistive load (b) Switching and output voltage waveform

The circuit operation is very simple since S1 and S2 are switched on and off alternatively at 50% duty cycle as shown in the switching waveform in Fig. 2.8 (b). This shows that the circuit generates a square ac voltage waveform across the load from a constant dc source. The voltages, V_{DC} and $-V_{DC}$ are across R when S1 ON while S2 OFF and when S2 is ON while S1 is OFF, respectively. One observation to be made here is that the frequency of the output voltage is equal to $f = 1/T$ and is determined by the switching frequency. This is true as long as S1 and S2 are switched complementarily. Moreover, the *rms* value of the output voltage is simply V_{DC}. Hence, to control the *rms* value of the output voltage we must control the rectified V_{DC} voltage source. Another observation is that the load power factor is unity since we have purely resistive load. That is rarely encountered in practical application.

Finally, we should note that in practice the above circuit does not require two equal dc voltage sources as shown in Fig. 2.8 (a). Instead, large splitting capacitors are used to produce two equal DC voltage sources [5].

The two capacitors are equal and very large so that RC is much larger than the half-switching period. This will guarantee that the mid-point, *a*, between the capacitors has a fixed potential at one-half of the supply voltage V_{DC} [5].

2.4.5 Inductive-Resistive Load

Figure 2.9 (a) shows a half-bridge inverter under inductive resistive load with the equivalent circuit and the output waveforms shown in Fig. 2.9 (b) and (c), respectively.

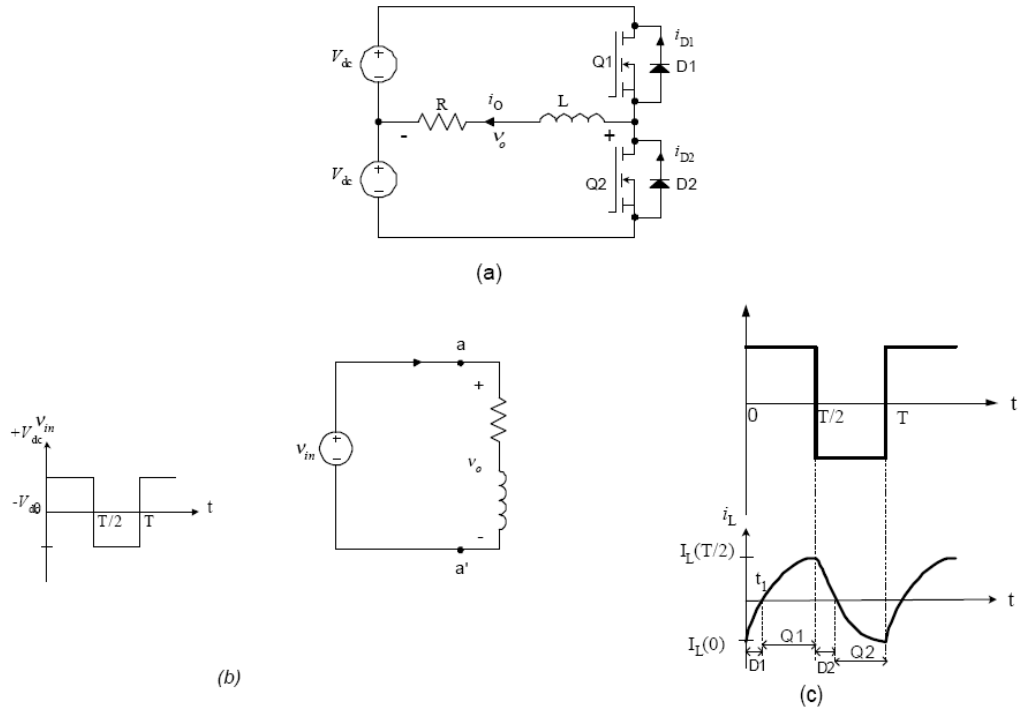

Figure 2.9 (a) Half-bridge inverter with inductive resistive load (b) Equivalent circuit and (c) Steady state waveforms.

With Q1 and Q2 switched complementary each at 50% duty cycle with switching frequency f , then the load between terminal a and $a¢$ is excited by square voltage waveform v (*t*) *in* of amplitudes $+V$ *dc* and $–V$ *dc* as shown in Fig. 2.9 (b), i.e. v (*t*) *in* is defined as follows:

$$v_{in}(t) = \begin{cases} +V_{dc} & 0 \le t < T/2 \\ -V_{dc} & T/2 \le t < T \end{cases} \qquad (2.2)$$

The switches are implemented by using conventional SCR (that require external forced commutation circuit) or fully controlled power switching devices such as IGBTs,

GTOs, BTJs or MOSFETs. Notice from the load current i_L direction, these switches must be bi-directional. Assume the inverter operates in steady state and its inductor current waveform is shown in Fig. 2.9(c) for 1 $0 < t < t$, *the* inductor current is negative which means while Q1 is ON the current actually flows in the reverse direction, i.e. in the body diode of the bi-directional switch Q1. At 1 $t = t$, the current flows through the transistor Q1 as shown. At $t = T$ 2, when S2 is turned ON, since the current direction is positive, the flyback diode, D2, turns ON until 1 $t = T$ 2 + t when Q2 starts conducting [5].

2.4.6 Sinusoidal PWM Waveforms

In Sinusoidal Pulse Width Modulation, SPWM, multiple pulses are generated, each having different width time. The width of each pulse is varied in proportion to the instantaneous integrated value of the required fundamental component at the time of its event. In other words, the pulse width becomes a sinusoidal function of the angular position. The repetition frequency of the output voltage will be a frequency higher than the fundamental. In applying SPWM, the lower order harmonics of the modulated voltage wave are highly reduced in contrast to the use of uniform pulse width modulation [5].

In SPWM the output voltage signal can be obtained by comparing a control signal, *cont v* , against a sinusoidal reference signal, *ref v* , at the desired frequency as shown in Fig 2.10. At the first half of the output period, output voltage takes a positive value (+ *dc V*), whenever the reference signal is greater than the control signal. At the same way, at the second half of the output period, the output voltage takes a negative value (- *dc V*) whenever the reference signal is less than the control signal [5].

The control frequency *cont f* determines the number of pulses per half of cycle for the output voltage signal. Also, the output frequency O_f is determined by the

reference frequency *ref f.* The modulation index Ma is defined as the ratio between the sinusoidal magnitude and the control signal magnitude [5].

To obtain a vary train of pulses, each pulse has to vary proportional to the necessary fundamental component precisely at the time when this pulse occurs. The frequency of the output waveform needs to be higher than the frequency of the fundamental component. By varying the width of each pulse, the inverter is able to produce different levels of output voltage for the corresponding pulse event [5].

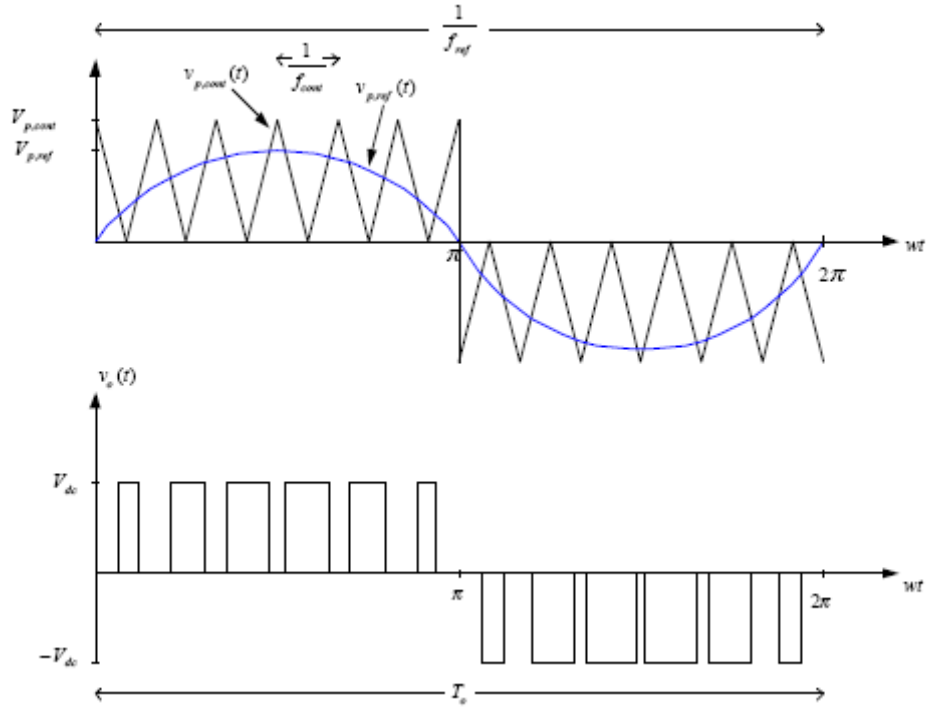

Figure 2.10: SPWM and Inverter Output Voltage.

CHAPTER 3

METHODOLOGY

3.1 Background

This chapter explains about hardware design for the inverter including PIC microcontroller circuit, H-bridge Inverter circuit and MOSFET driver circuit. This chapter also explains the calculation involve in designing the hardware.

Before looking at the detail of all the methods below, it is best to begin with brief review the correlation of all methods. The Figure 3.1 below show the correlation of all methods in this project.

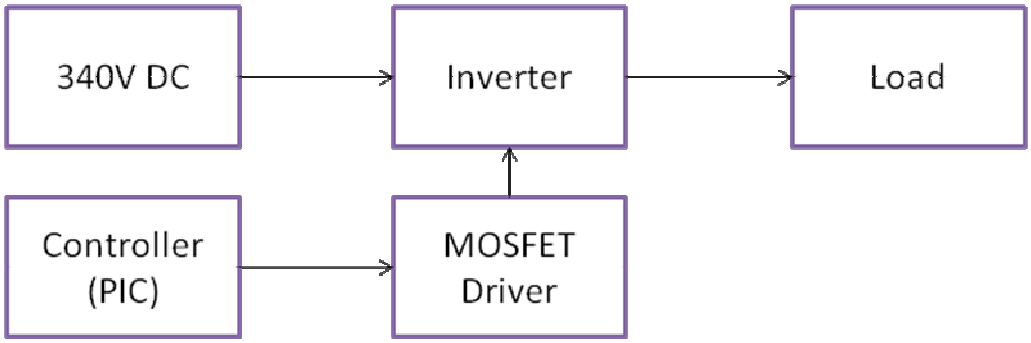

Figure 3.1: System design of Inverter system